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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/723,044	11/25/2003	Richard K. Errickson	POU920030189US1	7804
46429	7590 03/13/2006		EXAMINER	
011111	COLBURN LLP-IBM I ROAD SOUTH	NGUYEN, THAN VINH		
•• •	LD, CT 06002	ART UNIT	PAPER NUMBER	
	•		2187	
			DATE MAILED: 03/13/2006	

Please find below and/or attached an Office communication concerning this application or proceeding.

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	Application No.	Applicant(s)	
Office Action Commons	10/723,044	ERRICKSON ET AL.	
Office Action Summary	Examiner	Art Unit	
	Than Nguyen	2187	
The MAILING DATE of this communication app Period for Reply	ears on the cover sheet with the c	orrespondence address	
A SHORTENED STATUTORY PERIOD FOR REPLY WHICHEVER IS LONGER, FROM THE MAILING DA - Extensions of time may be available under the provisions of 37 CFR 1.13 after SIX (6) MONTHS from the mailing date of this communication. - If NO period for reply is specified above, the maximum statutory period w - Failure to reply within the set or extended period for reply will, by statute, Any reply received by the Office later than three months after the mailing earned patent term adjustment. See 37 CFR 1.704(b).	ATE OF THIS COMMUNICATION 36(a). In no event, however, may a reply be tim will apply and will expire SIX (6) MONTHS from cause the application to become ABANDONE	N. nely filed the mailing date of this communication. D. (35 U.S.C. § 133).	
Status			
Responsive to communication(s) filed on 11/25 2a) This action is FINAL. 2b) This 3) Since this application is in condition for alloware closed in accordance with the practice under E	action is non-final. nce except for formal matters, pro		
Disposition of Claims			
 4) □ Claim(s) 1-19 is/are pending in the application. 4a) Of the above claim(s) is/are withdraw 5) □ Claim(s) is/are allowed. 6) □ Claim(s) 1-19 is/are rejected. 7) □ Claim(s) is/are objected to. 8) □ Claim(s) are subject to restriction and/or 	vn from consideration.		
Application Papers			
9)☐ The specification is objected to by the Examiner 10)☒ The drawing(s) filed on 25 November 2003 is/ar Applicant may not request that any objection to the of Replacement drawing sheet(s) including the correction 11)☐ The oath or declaration is objected to by the Ex	re: a) \square accepted or b) \square object drawing(s) be held in abeyance. See on is required if the drawing(s) is obj	e 37 CFR 1.85(a). ected to. See 37 CFR 1.121(d).	
Priority under 35 U.S.C. § 119			
12) Acknowledgment is made of a claim for foreign a) All b) Some * c) None of: 1. Certified copies of the priority documents 2. Certified copies of the priority documents 3. Copies of the certified copies of the priority application from the International Bureau * See the attached detailed Office action for a list of the certified copies of the certified copies of the priorical purposes.	s have been received. s have been received in Applicati ity documents have been receive (PCT Rule 17.2(a)).	on No ed in this National Stage	
Attachment(s) 1) ☑ Notice of References Cited (PTO-892)	4) 🔲 Interview Summary	(PTO.413)	
Notice of References cited (PTO-892) Notice of Draftsperson's Patent Drawing Review (PTO-948) Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date 11/25/03,3/4/04.	Paper No(s)/Mail Da		

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DETAILED ACTION

1. Claims 1-19 are pending.

2. The IDSes, filed 11/25/03 and 3/4/04, have been considered.

Claim Rejections - 35 USC § 112

- 3. Claims 1-19 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.
- 4. As to independent claim 1, 13, 18, and 19 it is unclear as what is meant by "in accordance with a definition of a z/Architecture". It is unclear as how the definition of a z/Architecture is defined by the specification and how this definition relates to the claimed instructions. Is Applicant claiming the entire z/Architecture (a computing architecture) also or is the z/Architecture is an environment in which the invention operates? If the z/Architecture is an environment, it will not be given patentable weight. If the z/Architecture is a computing architecture is being claimed, Applicant must provide details of this architecture being claimed. Without knowing more details, one of ordinary skills cannot clearly understand the scope of the invention. Applicant is advised to clarify/define the phrase "a definition of a z/Architecture", without adding new matter.
- 5. Claims 2-12, 14-16 are also rejected for incorporating this deficiency.
- 6. Claim 8 and 15 recites the limitation "semiprivileged instructions" in line 2 of the claim. There is insufficient antecedent basis for this limitation in the claim. Applicant also did not define "semiprivileged instructions" in the specification.

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7. Claim 6 is rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the enablement requirement. The claim(s) contains subject matter which was not described in the specification in such a way as to enable one skilled in the art to which it pertains, or with which it is most nearly connected, to make and/or use the invention. It is unclear how an address space can alleviate use of the main address space. Where is this alleviation function defined for the address space? It appears that the alleviation is an expected result, not a function performed by the first address space. If it is an expected result, claim 6 does not further limit the parent claim since it does add more limitations/details to the parent claim.

Claim Objections

8. Claims 3-5 and 14 are objected to because of the following informalities: each of these claims is missing a period (.). Appropriate correction is required.

Claim Rejections - 35 USC § 102

- (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.
- 9. Claims 1-8,11-15,18,19 are rejected under 35 U.S.C. 102(e) as being anticipated by Bailey et al (US 6,598,144 B1).

 As to claims 1,6,13,18,19:
- 10. Bailey teaches the claimed system and method of performing memory mapped input output operations to an alternate address space comprising: establishing a first instruction directed to a first memory mapped input output alternate address space associated with an adapter to store data in accordance with a definition of a

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z/Architecture; establishing a second instruction directed to said first memory mapped

input output alternate address space associated with an adapter to load data in accordance

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with said definition(s) of said z/Architecture (send data instruction to adapter's MMIO;

4/25-32) (read data instruction to adapter's MMIO; 4/30-35); and wherein a process

issues at least one of said first instruction and said second instruction and thereby causes

execution of at least one of said store and load with said first alternate address space

(access to MMIO address space; 4/15-41).

As to claim 2:

11. Bailey teaches said first alternate address space is not a partition of a main address

space from which said issuing process is executing (adapter address space is separate

from system address space; 4/60-62).

As to claim 3:

12. Bailey teaches said process issuing said at least one of said first instruction and

said second instruction and thereby causes execution of at least one of said store and load

with said first alternate address space operates in a problem state of a machine (issue

read/write to MMIO address space in user mode; 2/11; 4/30-40).

As to claim 4:

13. Bailey teaches said execution includes said at least one of said store and load with

an allocated resources associated first alternate address space (4/15-41).

As to claim 5,14:

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14. Bailey teaches said problem state corresponds to a least privileged execution state

in said z/Architecture (user/kernel mode; 2/10-11).

As to claim 7:

15. Bailey teaches at least one of said first instruction and said second instruction is

executed without supervisory state intervention (user mode; 2/11).

As to claim 8,15:

16. Bailey teaches said first instruction and said second instruction are semiprivileged

instructions that may be executed in problem state, wherein ownership of a specified

resource of a specified adapter determines a privilege required for execution of said

semiprivileged instructions (user/kernel mode; 2/10-11).

As to claim 11:

Bailey teaches said adapter includes address spaces as partitions of said alternate address

space (MMIO/system address spaces; 4/60-65).

As to claim 12:

17. Bailey teaches said multiple address spaces are governed by at least one of a

resource type and storage area types associated with said adapter (system and MMIO

address spaces are for different resources; 4/55-65).

Claim Rejections - 35 USC § 103

18. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all

obviousness rejections set forth in this Office action:

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(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

19. Claims 9-10,16-17 are rejected under 35 U.S.C. 103(a) as being unpatentable over Bailey et al (US 6,598,144 B1).

As to claim 9,10,16,17:

20. Bailey does not specifically teach including a second alternate address space associated with a second adapter, the second alternate address space being different than the first alternate address space. Bailey only describes one host channel adapter with its MMIO address space. Bailey does teach operating in a system environment in which multiple host channel adapters are used (1/49-61). It would have been obvious to one of ordinary skills in the art at the time of the invention to use multiple host channel adapters, each with its own address space, in the invention of Bailey, to provide for more sharing of data across cluster resources, as suggested by Bailey.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Than Nguyen whose telephone number is 571-272-4198. The examiner can normally be reached on 8am-3pm M-F.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Than Nguyen can be reached on (571) 272-4201. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

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Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Than Nguyen Primary Examiner Art Unit 2187